WHAT IS CLAIMED IS:

1. A method, comprising:

identifying a setting for a capacitor bank associated with a voltage-controlled oscillator in a closed-loop phase-locked-loop, the setting representing a combination of one or more capacitors in the capacitor bank;

estimating a gain introduced by the closed-loop phase-locked-loop when the oscillator operates using the identified setting;

estimating a response of a loop filter in the phase-locked-loop;

identifying one or more coefficients for a digital filter using the identified gain and the identified loop filter response, the digital filter operable to filter an input signal; and

modulating the filtered input signal using the phase-locked-loop to produce an output signal.

2. The method of Claim 1, wherein identifying the setting for the capacitor bank comprises:

scaling the output signal produced by the voltage-controlled oscillator;

clocking a counter using the scaled output signal to produce a counter signal;

estimating a frequency of the counter signal a plurality of times;

identifying differences between the estimated frequencies and a desired frequency;

accumulating the differences;

filtering the accumulated differences; and

processing the filtered accumulated differences to produce the setting for the capacitor bank.

3. The method of Claim 1, wherein estimating the gain introduced by the closed-loop phase-locked-loop comprises:

setting a desired frequency associated with the phase-locked-loop to a first value;

identifying a first input value to a digital-to-analog converter in a charge pump in the phase-locked-loop;

setting the desired frequency to a second value;

identifying a second input value to the digital-to-analog converter;

identifying a difference between the first and second input values; and

identifying the gain of the phase-locked-loop using the identified difference.

4. The method of Claim 3, wherein the identified gain comprises an estimated unity gain bandwidth; and

further comprising:

identifying an ideal input value for the digital-to-analog converter;

rounding down the ideal input value to generate an actual input value; and

identifying an actual gain introduced by the phase-locked-loop using the actual input value.

5. The method of Claim 4, wherein estimating the response of the loop filter comprises:

identifying an error between the ideal input value for the digital-to-analog converter and the actual input value; and

estimating the response of the loop filter using the identified error.

6. The method of Claim 1, wherein identifying the one or more coefficients for the digital filter comprises:

identifying a transfer function from the input signal to the output signal;

transforming the transfer function to generate a transformed transfer function; and

calculating one or more values for the one or more coefficients using the transformed transfer function.

7. The method of Claim 1, wherein the digital filter alters the input signal to at least partially compensate for an irregularity introduced into the output signal by the closed-loop phase-locked-loop.

8. The method of Claim 1, wherein:

the phase-locked-loop and the digital filter form at least a portion of a frequency synthesizer;

the frequency synthesizer occupies no more than 4 mm^2 of space;

the frequency synthesizer operates using no more than 35 mA of current; and

the estimating steps, the identifying steps, and a time needed for the phase-locked-loop to settle collectively take no more than 140 μs.

9. A frequency synthesizer, comprising:

a digital filter operable to receive and filter an input signal;

a closed-loop phase-locked-loop comprising a voltage-controlled oscillator and a loop filter, the phase-locked-loop operable to receive the filtered input signal and generate an output signal; and

a controller operable to:

identify a setting for a capacitor bank associated with the voltage-controlled oscillator, the setting representing a combination of one or more capacitors in the capacitor bank;

estimate a gain introduced by the phase-locked-loop when the oscillator operates using the identified setting;

estimate a response of the loop filter;

identify one or more coefficients for the digital filter using the identified gain and the identified loop filter response.

10. The frequency synthesizer of Claim 9, wherein the controller is operable to identify the setting for the capacitor bank by receiving the setting from a capacitor select circuit, the capacitor select circuit comprising:

a prescaler operable to scale the output signal produced by the voltage-controlled oscillator;

a counter operable to be clocked by the scaled output signal to produce a counter signal;

a digital frequency discriminator operable to estimate a frequency of the counter signal a plurality of times;

an adder operable to identify differences between the estimated frequencies and a desired frequency;

an integrator operable to accumulate the differences;

a low-pass filter operable to filter the accumulated differences; and

an averaging unit operable to average the filtered accumulated differences to produce the setting for the capacitor bank.

11. The frequency synthesizer of Claim 9, wherein the controller is operable to estimate the gain by:

setting a desired frequency associated with the phase-locked-loop to a first value;

identifying a first input value to a digital-to-analog converter in a charge pump in the phase-locked-loop;

setting the desired frequency to a second value;

identifying a second input value to the digital-to-analog converter;

identifying a difference between the first and second input values; and

identifying the gain of the phase-locked-loop using the identified difference.

12. The frequency synthesizer of Claim 11, wherein:

the identified gain comprises an estimated unity gain bandwidth; and

the controller is further operable to estimate the gain by:

identifying an ideal input value for the digital-to-analog converter;

rounding down the ideal input value to generate an actual input value; and

identifying an actual gain of the phase-locked-loop using the actual input value.

13. The frequency synthesizer of Claim 12, wherein the controller is operable to estimate the response of the loop filter by:

identifying an error between the ideal input value for the digital-to-analog converter and the actual input value; and

estimating the response of the loop filter using the identified error.

14. The frequency synthesizer of Claim 9, wherein the controller is operable to identify the one or more coefficients for the digital filter by:

identifying a transfer function from the input signal to the output signal;

transforming the transfer function to generate a transformed transfer function; and

calculating one or more values for the one or more coefficients using the transformed transfer function.

15. The frequency synthesizer of Claim 9, wherein the digital filter alters the input signal to at least partially compensate for an irregularity introduced into the output signal by the closed-loop phase-locked-loop.

16. The frequency synthesizer of Claim 9, wherein:

the frequency synthesizer occupies no more than 4 mm^2 of space;

the frequency synthesizer operates using no more than 35 mA of current; and

the frequency synthesizer is operable to perform the estimating and the identifying functions and the phase-locked-loop is operable to settle collectively within no more than 140 μs.

17. A wireless device, comprising:

an antenna operable to transmit outgoing signals over a wireless interface; and

a transceiver operable to generate the outgoing signals, the transceiver comprising a frequency synthesizer, the frequency synthesizer comprising:

a digital filter operable to receive and filter an input signal;

a closed-loop phase-locked-loop comprising a voltage-controlled oscillator and a loop filter, the phase-locked-loop operable to receive the filtered input signal and generate the outgoing signal; and

a controller operable to:

identify a setting for a capacitor bank associated with the voltage-controlled oscillator, the setting representing a combination of one or more capacitors in the capacitor bank;

estimate a gain introduced by the phase-locked-loop when the oscillator operates using the identified setting;

estimate a response of the loop filter; and

identify one or more coefficients for the digital filter using the identified gain and the identified loop filter response.

18. The wireless device of Claim 17, wherein the controller is operable to identify the setting for the capacitor bank by receiving the setting from a capacitor select circuit, the capacitor select circuit comprising:

a prescaler operable to scale the outgoing signal produced by the voltage-controlled oscillator;

a counter operable to be clocked by the scaled outgoing signal to produce a counter signal;

a digital frequency discriminator operable to estimate a frequency of the counter signal a plurality of times;

an adder operable to identify differences between the estimated frequencies and a desired frequency;

an integrator operable to accumulate the differences;

a low-pass filter operable to filter the accumulated differences; and

an averaging unit operable to average the filtered accumulated differences to produce the setting for the capacitor bank.

19. The wireless device of Claim 17, wherein the controller is operable to estimate the gain and the response by:

setting a desired frequency associated with the phase-locked-loop to a first value;

identifying a first input value to a digital-to-analog converter in a charge pump in the phase-locked-loop;

setting the desired frequency to a second value;

identifying a second input value to the digital-to-analog converter;

identifying a difference between the first and second input values;

estimating a unity gain bandwidth of the phase-locked-loop using the identified difference;

identifying an ideal input value for the digital-to-analog converter;

rounding down the ideal input value to generate an actual input value;

identifying an actual gain of the phase-locked-loop using the actual input value;

identifying an error between the ideal input value for the digital-to-analog converter and the actual input value; and

estimating the response of the loop filter using the identified error.

20. The wireless device of Claim 17, wherein the controller is operable to identify the one or more coefficients for the digital filter by:

identifying a transfer function from the input signal to the outgoing signal;

transforming the transfer function to generate a transformed transfer function; and

calculating one or more values for the one or more coefficients using the transformed transfer function.